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PTO/SB/08A (08-00)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

Complete If Known	
Application Number	09/847,642
Filing Date	May 1, 2001
First Named Inventor	Mihai T. Lazarescu
Group Art Unit	[redacted] 2124
Examiner Name	[redacted] INGBERG
Attorney Docket Number	261/246

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
TI	AA	Prof. Dov Dori, About OPCAT, 2000, pages 1-2, http://iew3.technion.ac.il~dori/opcat/about.htm1	
TI	AB	Prof. Dov Dori, OPM Methodology, 2000, pages 1-3, http://iew3.technion.ac.il/~dori/opcat/methodology.htm1	
TI	AC	Prof. Dov Dori; OPCAT's Contents, 2000, pages 1-5, http://iew3.technion.ac.il~dori/opcat/contents.htm1	
TI	AD	Prof. Dov Dori; Examples; 2000, pages 1-3 http://iew3.technion.ac.il/~dori/opcat/example.htm1 **(Fig. 1 and Fig. 2 did not display when website was viewed).**	
TI	AE	Vojin Zavojnovic, Stefan Pees, Christian Schlaeger, Markus Willems, Rainer Schoenen and Heinrich Meyr; DSP Processor/Complier Co-Design A quantitative Approach, ICSPAT, 1997, pages 761 - 765	
TI	AF	Guido Post, Vojin Zivonjovic and Sebastian Ritz; Multiprocessor, Architecture Extension for the BlockDiagram-Oriented Design Tool Cossap/Descartes, ICSPAT, 1995	
TI	AG	Stefan Pees, Vojin Zivojnovic, Andreas Hoffmann, Heinrich Meyr; Retargetable Timed Instruction Set Simulation of Pipelined Processor Architectures , ICSPAT, 1998	
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TI	AJ	Graham R. Hellestrand, Designing System on a Chip Products Using Systems Engineering Tools, 1999, pages 1-6, VaST Systems Technology Corporation	
TI	AK	Vojin Zivojnovic, Stefan Pees, Heinrich Meyr, LISA - Machine Description Language and Generic Machine Model for HW/SW Co-Design, October 1996, 1996 IEEE Workshop on VLSI Signal Processing, San Francisco	
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TI	AQ	Dr. Graham Hellestrand, The Advent of the Virtual Processor Model, E. E. Times, May 14, 1999, pages 1-7, VaST Systems Technology, Santa Clara, CA, USA	
TI	AR	Graham R. Hellestrand, Systems Engineering: The Era of the Virtual Processor Model (VPM), April 14, 1999, pages 1-6, VaST Systems Technology, Santa Clara, CA, USA	
TI	AS	Stephan Ohr, Neolinear Tips Analog Synthesis, E. E. Times, June 12, 2001, Pages 1-3, Com, http://www.eetimes.com/story/OEG20010612S0067	

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Examiner Name	[redacted] I UGUBERG
Attorney Docket Number	261/246

TR	AT	Soner Önder, Rajiv Gupta, Automatic Generation of Microarchitecture Simulators, May 1998, IEEE International Conference on Computer Languages	
TF	AU	Joachim Fitzner, ChrisSchläger, Davorin Mista, Vojin Zivojnovic, Implementing LISA Tools Based on a DSP Architecture Description, ICSPAT 1999	
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TI	AX	Chris Schlager, Joachim Fitzner, Vojin Zivojnovic, Using Supersim Complied Processor Models for Hardware, Software and System Design, ICSPAT 1998	
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Examiner Signature		Date Considered	4/14/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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